

# Design Margin Testing (HALT)

## Introduction

In order to increase the field reliability of its power supplies, Condor uses HALT (*Highly Accelerated Life Test*), testing. This is a design margin test, where the test specimen is exposed to successively higher levels of stress, until failure occurs. The failure mechanism is diagnosed, corrected, and the process is repeated until an acceptable level of margin is achieved. An acceptable level is usually a point where the design limit is reached, or implementation of a fix is technically or economically unfeasible. The stress can be vibration, temperature, temperature cycling, input voltage, output load, or any stimulus, which induces a relevant failure. The levels used in the testing always exceed the maximum design requirements, so by definition, a level of margin is being demonstrated. The greater the design margin, the less likely that a field failure will occur due to that particular stimulus.

In addition, this testing can be performed in a short time frame, due to the *acceleration factor* achieved by higher stress levels.

## Theory

The failures precipitated by this type of testing generally fall into four categories:

- Workmanship - Assembly errors, which are always fixed, and the test continued.
- Design Deficiency - A weakness in the product design
- Component Limit - The maximum stress of a component is exceeded.
- Fatigue - The cumulative effect of many stress reversals.

For power electronics, an additional failure mode needs to be addressed:

- “Non-linear” - In power electronics at elevated temperatures, the power dissipation of a unit can, over time, increase in a type of positive feedback, resulting in a “thermal runaway”. To verify this, a 6 hour soak at 60°C, with 3 hours at high line and 3 hours at low line is included in the test.

The acceleration factor for mechanical fatigue is often given by Miner’s Rule:

$$CD = n\sigma^a$$

where:

CD = cumulative damage

n = number of cycles

s = stress level

a = exponent derived from S/N curve (Stress vs. Number of cycles curve, used to determine fatigue life) a material, typically 5.5 - 7.5 for most electronic equipment materials

Therefore, for an equivalent time, the vibration acceleration factor is:

$$AF_{vib} = \left( \frac{g'_{rms}}{g_{rms}} \right)^a$$

where:

AF<sub>vib</sub> = Vibration acceleration factor

g'<sub>rms</sub> = Vibration level 2 in g<sub>rms</sub> (g=32.2 ft/sec<sup>2</sup>=9.81 m/s<sup>2</sup>)

g<sub>rms</sub> = Vibration level 1 in g<sub>rms</sub>

For example, a 10 g<sub>rms</sub> vibration level produces 90 times the damage of a 5 g<sub>rms</sub> level using an a=6.5. This mechanism also applies to the stresses induced by Thermal Coefficient of Expansion mismatches during temperature cycling.

The acceleration factor for elevated temperature typically uses the Arrhenius Model:

$$A.F. = e^{\left(\frac{E}{K}\right)\left(\frac{1}{T_1} - \frac{1}{T_0}\right)}$$

Where:

$T_1$  = Normal Ambient Temp. (298 °K)

$T_0$  = Elevated Ambient Temp (°K)

E = Activation Energy (.825 eV, Typ.)

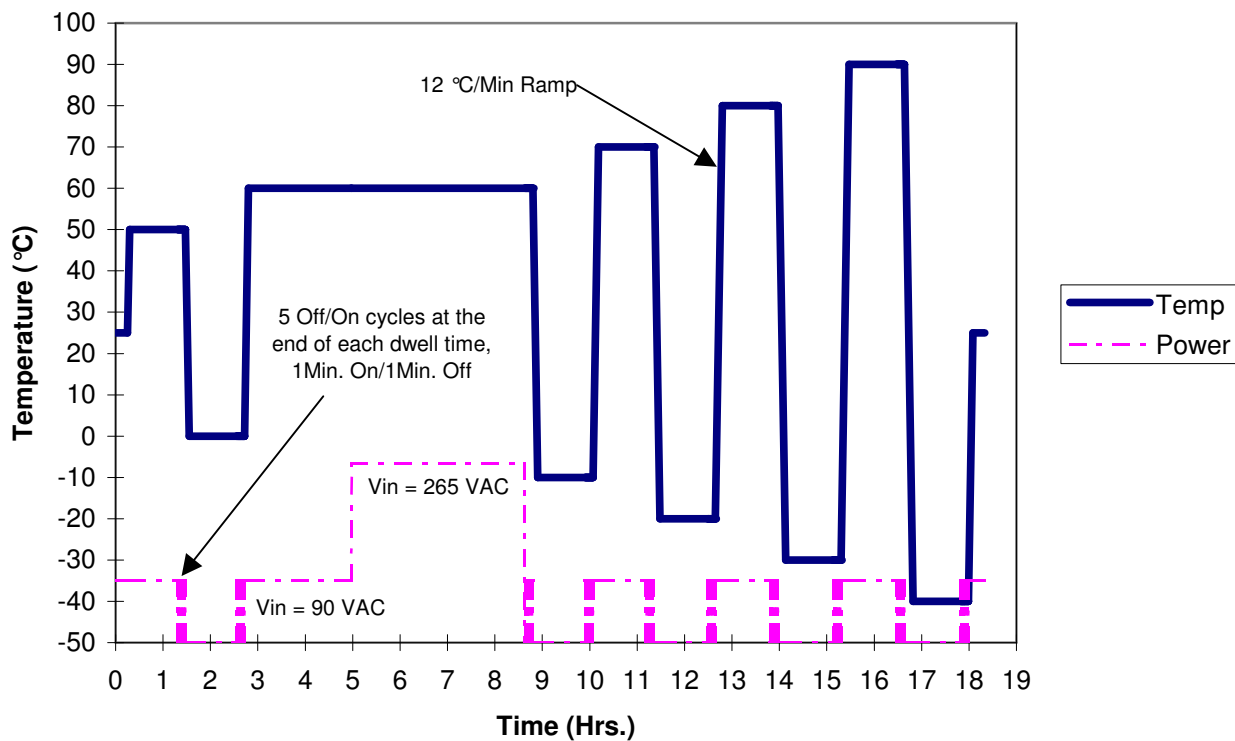
K = Boltzman's constant

Hence, an ambient temperature of 60°C yields an acceleration factor of 30 over a normal 25°C ambient.

### Thermal HALT Test

1. Disable thermal protection and perform functional test
2. Attach thermocouples (as required), and monitor line input Vac, output Vdc, and other signals as necessary, with data acquisition unit.
3. Perform temperature cycling per Figure 1.
4. Perform functional test
5. Determine root cause of any failures, implement corrective action (if required), and repeat test (if required).
6. Generate report.

**Condor Temperature HALT Profile (Figure 1)**



## Vibration HALT Test

1. Perform functional test
2. Attach response accelerometers (if required), and monitor output Vdc to determine when the unit fails.
3. Perform 5 levels of vibration testing in each of three axes per Table 1.
4. Perform functional test
5. Determine root cause of any failures, implement corrective action (if required), and repeat test (if required).
6. Generate report.

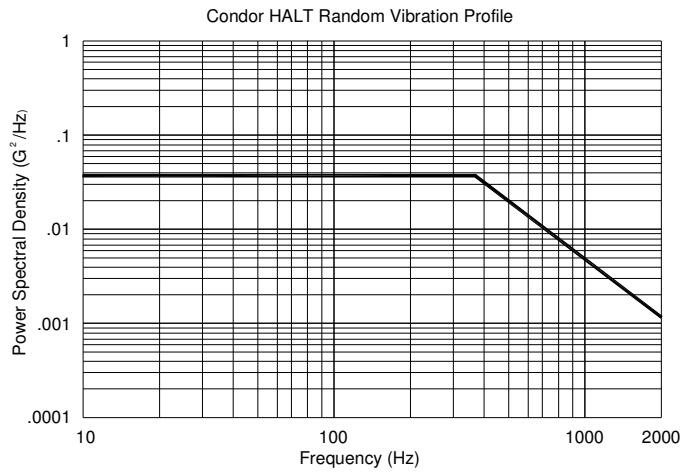


Table 1

Level	Time (Min:Sec)	Overall G <sub>rms</sub>	PSD G <sup>2</sup> /Hz		
			10 Hz	350 Hz	2000 Hz
1	10:00	5	0.038	0.038	0.0012
2	10:00	7	0.078	0.078	0.0024
3	10:00	9	0.129	0.129	0.004
4	10:00	11	0.192	0.192	0.0059
5	10:00	13	0.269	0.269	0.0082